6. THE CLAIMS

It is claimed:

1. A data strobe receiver comprising:

a) a first comparator, the first comparator having a first input that is coupled to a first reference voltage, the first comparator having a second input that is coupled to a data strobe, the first comparator having an output;

b) a delay element, the delay element having an input that is coupled to the output of the first comparator;

c) a second comparator, the second comparator having a first input that is coupled to a second voltage reference, the second comparator having a second input that is coupled to the data strobe, the second comparator having an output; and

d) a divide-by-X-counter, where X is an integer greater than 1 and less than 129, the divide-by-X-counter having an input that is coupled to the output of the second comparator.

2. The data strobe receiver of claim 1, wherein the delay element includes an enable input.

3. The data strobe receiver of claim 1, wherein the delay element delays the output of the first comparator by more than 45 degrees.

4. The data strobe receiver of claim 1, wherein the delay element delays the output of the first comparator by less than 135 degrees.

5. The data strobe receiver of claim 1, wherein the delay element delays the output of the first comparator by more than 45 degrees and less than 135 degrees.

6. The data strobe receiver of claim 1, wherein the delay of the delay element is programmable.

7. The data strobe receiver of claim 1, wherein the value of X is programmable.

8. The data strobe receiver of claim 1, wherein a divide-by-X-counter has an inverted reset input.

9. The data strobe receiver of claim 1, wherein the divide-by-X-counter includes an inverted output.

10. The data strobe receiver of claim 1, wherein the divide-by-X-counter is a divide-by-4-counter.

11. The data strobe receiver of claim 1, further comprising:

e) a set-reset-flip-flop, the set-reset-flip-flop having an input that is coupled to the output of the second comparator.

12. The data strobe receiver of claim 11, wherein the input that is coupled to the output of the second comparator is an inverted set input.

13. The data strobe receiver of claim 11, wherein the set-reset-flip-flop contains an output that is coupled to the input of a first AND gate.

14. The data strobe receiver of claim 11, wherein the data strobe receiver contains a first AND gate, the set-reset-flip-flop contains an output that is coupled to the first input of the first AND gate, and the divide-by-X-counter contains an inverted reset input that is coupled to the first input of the first AND gate.

15. The data strobe receiver of claim 11, wherein the data strobe receiver contains a first OR gate, the first OR gate having a first input and a second input, the first input of the first OR gate is coupled to the inverted output of the divide-by-X-counter, and the second input of the first OR gate is coupled to the output of the delay element.

16. The data strobe receiver of claim 15, wherein the data strobe receiver contains a second OR gate having a first input and a second input, the first input of the second OR gate is coupled to a continuous read signal, and the second input of the second OR gate is coupled to the output of the first OR gate.

17. The data strobe receiver of claim 16,wherein the set-reset-flip-flop includes an inverted reset input.

18. The data strobe receiver of claim 16, wherein the set-reset-flip-flop includes an inverted reset input, and the second OR gate includes an output that is coupled to the inverted reset input of the set-reset-flip-flop via a second AND gate.

19. The data strobe receiver of claim 18, wherein the second AND gate contains a first input and a second input, the first input of the second AND gate is coupled to a reset signal and the second input of the second AND gate is coupled to the output of the second OR gate.

20. The data strobe receiver of claim 18, wherein the second AND gate contains a first input and a second input, the first input of the second AND gate is coupled to an inverted output enable signal and the second input of the second AND gate is coupled to the output of the second OR gate.

21. The data strobe receiver of claim 18, wherein the second AND gate contains a first input, a second input, and a third input, the first input of the second AND gate is coupled to a reset signal, the second input of the second AND gate is coupled to the output of the second OR gate, and the third input of the second AND gate is coupled to an inverted output enable signal.

22. The data strobe receiver of claim 1, wherein the output of the delay element is coupled to an insert input of a first-in-first-out buffer.

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